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A Proposed Wallace Tree Multiplier Using Full Adder and Half Adder

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Abstract: The power management has become a great concern due to the increased usage of multimedia devices. Multipliers are the main sources of power consumption in these devices. Multipliers based on Wallace reduction tree provide an area-efficient strategy for high speed multiplication. The adder circuit is used as a main component in the multiplier circuits. A number of modifications are proposed in the literature to optimize the area of the Wallace multiplier.A Wallace tree multiplier is a fast multiplies utilize full and half adder in the decrease stage. As far as range and power the execution of XOR-XNOR gates and MUX effective. The proposed method Wallace tree multiplier is far better compare to traditional method.

Keywords: Wallace tree multiplier, Multiplexer, Full adder, Half adder, Cadence tool.

I. INTRODUCTION

A multiplier plays a vital role in any digital signal processors. There are different methods and architectures for designing a multiplier. Designing a multiplier by using wallace tree architecture is superior over other architectures in terms of performance characteristics. A multiplier designed by using wallace tree architecture is known as a wallace multiplier. Wallace multiplier consumes less power and its switching speed is faster as compared to other multiplier architectures. Researchers have shown interest on wallace multiplier, as result of which, different architectures are introduced to design a better wallace multiplier architecture. A conventional wallace multiplier and a reduced complexity wallace multiplier are two architectures among them. In this paper design and performance analysis of a conventional wallace multiplier and a reduced complexity wallace multiplier are discussed. Performance analysis is carried out by using Cadence Virtuoso in 180nm CMOS technology.

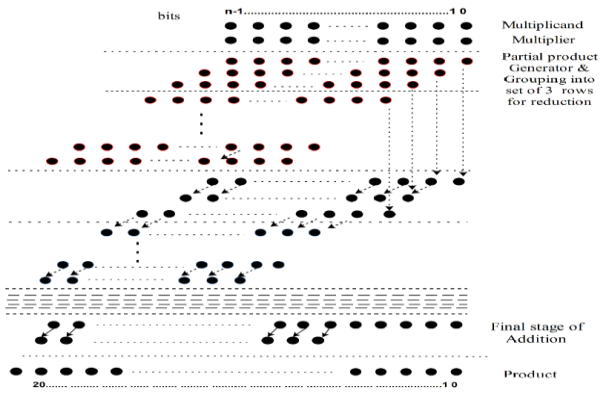

Figure 1:Wallace tree multiplier Structure

These 3 rows are summed using FAs and if there are 2 dots in a particular column, half adders are used. The resulting sum and carry signals from the half and full adders are passed to the next stage. The process is repeated till all the n partial product are summed. The resulting sum and carry out of the last stage is added using a fast carry propagation adder at the final stage.

In the proposed technique the problastic gate level force estimation are utilized to assess the power in the every stage. To decrease the switching activity the generation of partial product item should reordered which is additionally a lead to reduction in power. The partial product items is gets distributed into four gathering. The dada gathering is gets connected to one gathering and Wallace multiplier is connected to another gathering to accomplish low power utilization.

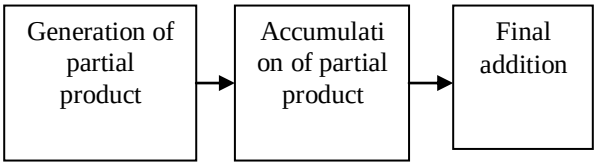

Figure 2: Block diagram of Wallace tree multiplier

Fig. 2 shows the block diagram of a wallace multiplier. In this multiplier architecture, after generating the partial product, accumulation of partial product and final addition are done in different stages. When the final stage obtains only two rows, then final addition is done. The number of rows of partial product in a particular stage can be expressed as Ri+1 = 2(Ri /3)+ Ri mod 3 where, Ri gives the groups or stages and R0 = N= number of bits. Let us consider an example that N bits multiplication, N2 AND gates are required to generate the partial product terms and the number of reduction stages is given by S

$$s = \log 2^{N}$$

The hardware requirements is done in terms of full adder (FA) and the length of final adder (FAL) for diifernt size

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of Wallace multiplier is obtained. A fast process for multiplication of two numbers was developed by Wallace. By using the Wallace method, a three step process is used for the multiplication of two numbers; the bit products are formed.

II. CONVENTIONAL FULL ADDER

In a conventional wallace multiplier, partial products are generated first. Then these are accumulated in different stages. The procedure is repeated until last stage contains only two rows. A 4x4 bit conventional wallace multiplier is designed by using Cadence virtuoso in 180nm CMOS technology. The flowchart for designing a conventional wallace multiplier is shown in Fig. 2.Design of the conventional Wallace multiplier is done in three steps: i) Partial product generation ii) Accumulation of partial product iii) Final addition

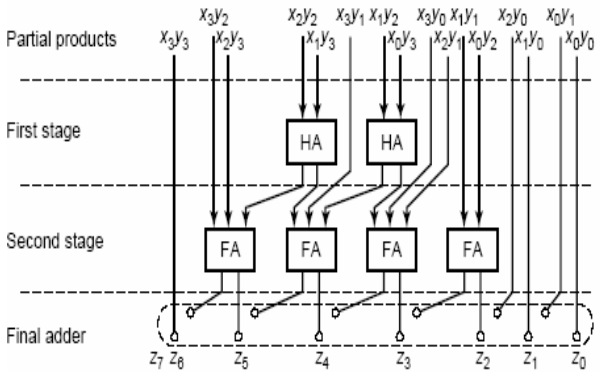
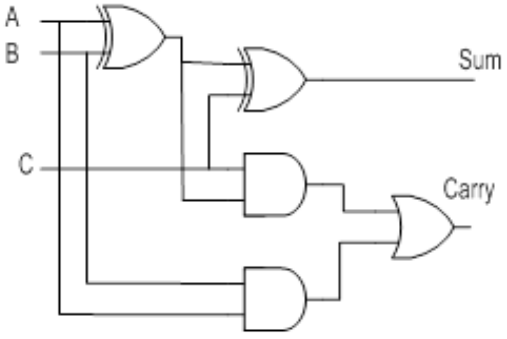


Figure 2: Conventional Wallace tree multiplier

In the reduction phase the conventional Wallace tree multiplier uses full adder high power consumption is caused due to bottleneck of full adder. The conventional full adder is shown in the below figure (3).



Fiureg.3 . Full adder

The above figure consists of two XOR gate and two AND gate and one OR gate. Here the main criteria is high power consumption and also includes increased in area. The critical path delay can be calculated as

$$\text{Delay} = 2 * \text{XOR}\,\Delta$$

The objective of the project is to In this paper The proposed and the existing multiplier designs are developed using Verilog HDL for 8 and 16 bits, respectively. The functionality of the 8-bit proposed Wallace tree multiplier is verified through simulations using cadence tool.

III. PROPOSED METHOD

In MUX based full adder the full adder is implemented using 4:1 multiplexers as shown in fig. 3. By implementing MUX based full adder in reduction phase of Wallace tree multiplier power reduction has been achieved.

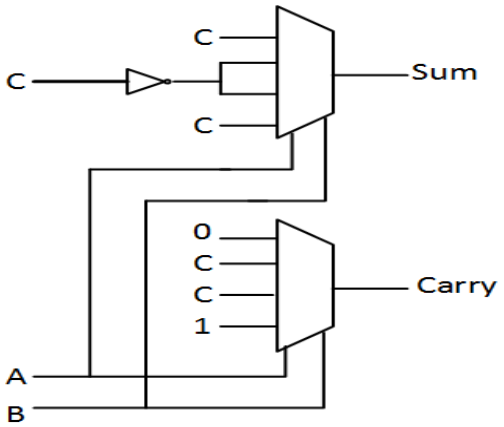


Figure 4: 4:1 MUX based Full Adder

In order to reduce the power and area, the conventional full adder in reduction phase of Wallace tree multiplier is replaced by a modified full adder. It is evident that, one 4:1 MUX can be made using three 2:1 MUX. The critical path delay can be written as shown in figure 4

$$\text{Delay} = \text{NOT}\Delta + 2 * \text{MUX}\Delta$$

The Wallace tree multiplier can be made more efficient by further reducing the critical path delay. The same can be achieved by using proposed full adder.
Each multiplexer has been realized by using two transistors, for the realization of the full adder circuit. The major source of power dissipation in any circuit is short circuit current, leakage current and logic transition. Since in this circuit there is no probability of direct path formation between source and ground.

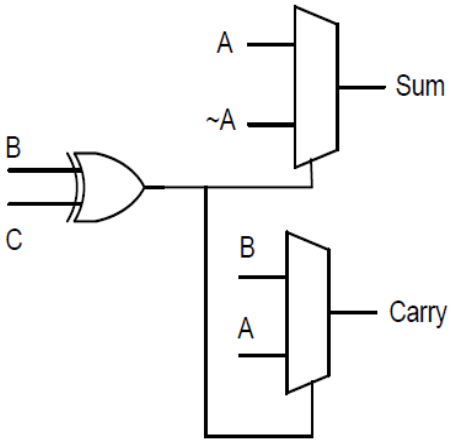


Figure 5: Proposed full adder

In Wallace tree structure the partial products is divided into certain levels. In each level, whenever there are three bits, full adder has to be used. Out of the three inputs, one input and its complement is provided as inputs to the first multiplexer. The other two inputs are given to XOR gate,

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the output of which will act as a select line to both the multiplexers.The inputs of the second multiplexer are, the bits other than the carry bit. This unique way of designing leads to the reduction of the switching activity, which in turn reduces the power. In addition to this, the critical path delay is also reduced compared to the existing designs discussed in literature, which leads to reduction in delay and thus increasing the speed. Operation of the proposed full adder can be explained as follows:

a) When B and C = 0 or 1 then sum = A;
b) When B = 0 or C = 1 vice versa then sum=A;
c) When B and C = 0 or 1 carry= B;
d) When B = 0 or C = 1 vice versa then carry=A.

IV. SIMULATION RESULT

Area:

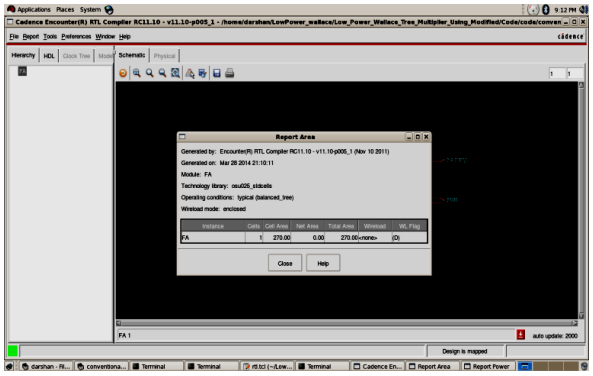

Figure 6: Area of Wallace tree multiplier

Power:

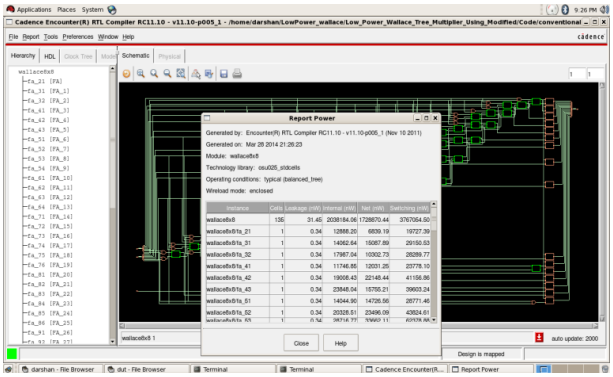

Figure 6: Power of Wallace tree multiplier

Delay:

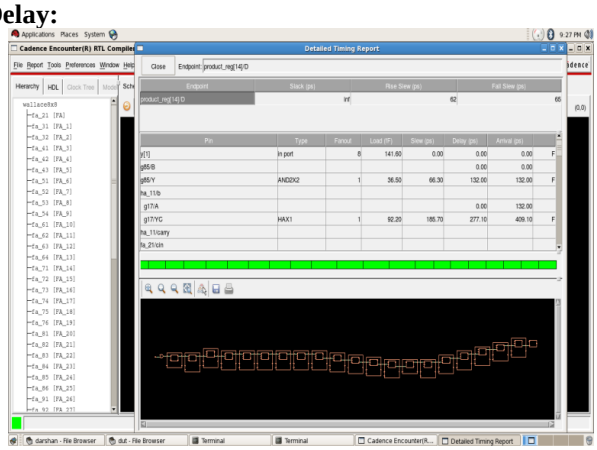

Figure 7: Delay of Wallace tree multiplier

Table1: Results

	Area(μm^2)	Power(mW)	Delay(ns)
Conventional Full adder (16 bits)	12174.5	7.19	8.23
Proposed full adder(16 bits)	11627.71	6.62	8.82

V. CONCLUSION

In this paper, a multiplexers using full adder of Wallace tree multiplier and XOR gate gets modified so that the area can be reduced. In reduction phase by implementing a modified full adder of Wallace tree an average power, area and delay is reduced, compared to existing methods respectively is achieved. The synthesis result confirms that the proposed Wallace tree multiplier is suitable for low power and small area applications. The designs are synthesized in using Cadence tool RTL complier.

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